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EXAMINER	
BURLESON, MICHAEL L	
ART UNIT	**PAPER NUMBER**
2626	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,649	FUKUDA ET AL.	
	Examiner	Art Unit	
	Michael Burleson	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3,7-15*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims1,4,5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawai et al. US 5715436.

Regarding claim 1, Kawai et al. teaches of a programmable processor (image processing LSI circuit), adaptable to three image processing steps, that process image information (column 2, lines 43-45), which reads on a programmable image processing unit which processes image data as a visualized image, the image data represented by a digital signal generated based on an image, and allows realization of a plurality of image formation operations. He teaches of a data memory M1 (column 9,lines 2-4), which reads on an image data storage unit that stores the image data. Kawai et al. teaches of an image processing LSI circuit (1) which outputs a read address signal, which tells the data memory M1 to output image data V1 to the image processing LSI circuit (1) (column 2, lines 3-5), which reads on an image data storage management unit which manages access to said image data storage section. He teaches an image processing LSI circuit (1) that receives image data from data memory M1 (column 9,

lines 27-30), which reads on an image data transmission of the image data between a data bus transmitting the image data and a processing unit used for the image processing conducted by said image processing unit. Kawai et al. teaches of a SIMD type first to third processing units (column 9,lines 53-54), which reads on a SIMD type data operation unit. He also teaches that SIMD type first to third processing units generate address signal (29) for data memories 2-1 – 2-3 (column 9, lines 56-59), which reads on a plurality of memories used for the image processing conducted by said SIMD type data operation unit. Kawai et al. teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 and external memories M1 to M3 (column 9, lines 59-62), which reads on a memory controller controlling said plurality of memories. He also teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 (column 9, lines 59-62), which reads on a memory switch controlling connection of said plurality of memories. Kawai et al. shows data lines 25-1 –25-3, 26-1 – 26-3 which transfer data to the image processing units 1-1 – 1-3 (column 10, lines 43-50), which reads on a plurality of data buses for inputting and outputting the image data. He teaches of selector circuits (40-1 and 40-2) (column 10, lines 36-50 and figure 5), which reads on a bus switch controlling connection between said plurality of data buses and said data operation unit. He also teaches of a post processing portion which performs a second image processing (column 10, lines 24-27), which reads on at least one auxiliary operation unit which assists said data operation unit.

3. Regarding claim 4, Kawai et al. teaches of a post processing portion (5) referred to a second image processing (column 10, lines 24-27) and image processing LSI circuit (1) that performs a third image processing step (column 9, lines 34-36), which reads on a plurality of auxiliary operations units are provided and at least one of auxiliary operation units has a non-SIMD type constitution for executing a consecutive operation processing.

Regarding claim 5, claim 5 is rejected for the same reasons as claim 1.

Regarding claim 8, claim 8 is rejected for the same reasons as claim 4.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2,3,6,7,9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. US 5715436 in view of Harney US 5522080.

Regarding claim 2, Kawai et al. teaches of a programmable processor (image processing LSI circuit), adaptable to three image processing steps, that process image information (column 2, lines 43-45), which reads on a programmable image processing unit which processes image data as a visualized image, the image data represented by a digital signal generated based on an image, and allows realization of a plurality of

image formation operations. He teaches of a data memory M1 (column 9,lines 2-4), which reads on an image data storage unit that stores the image data. Kawai et al. teaches of an image processing LSI circuit (1) which outputs a read address signal, which tells the data memory M1 to output image data V1 to the image processing LSI circuit (1) (column 2, lines 3-5), which reads on an image data storage management unit which manages access to said image data storage section. He teaches an image processing LSI circuit (1) that receives image data from data memory M1 (column 9, lines 27-30), which reads on an image data transmission of the image data between a data bus transmitting the image data and a processing unit used for the image processing conducted by said image processing unit. Kawai et al. teaches of a SIMD type first to third processing units (column 9,lines 53-54), which reads on a SIMD type data operation unit. He also teaches that SIMD type first to third processing units generate address signal (29) for data memories 2-1 – 2-3 (column 9, lines 56-59), which reads on a plurality of memories used for the image processing conducted by said SIMD type data operation unit. Kawai et al. teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 and external memories M1 to M3 (column 9, lines 59-62), which reads on a memory controller controlling said plurality of memories. He also teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 (column 9, lines 59-62), which reads on a memory switch controlling connection of said plurality of memories. Kawai et al. shows data lines 25-1 –25-3, 26-1 – 26-3 which transfer data to the image processing units 1-1 – 1-3 (column 10, lines 43-50),

which reads on a plurality of data buses for inputting and outputting the image data. He teaches of selector circuits (40-1 and 40-2) (column 10, lines 36-50 and figure 5), which reads on a bus switch controlling connection between said plurality of data buses and said data operation unit. He also teaches of a post processing portion which performs a second image processing (column 10, lines 24-27), which reads on at least one auxiliary operation unit which assists said data operation unit.

6. Kawai et al. fails to teach of the memory controller and memory switch selectively connect any one or more memories to the data operation unit.

7. Harney teaches of a block transfer controller (368) (column 13, lines 31-40), which reads on a memory controller and a memory interface (370) (column 13, lines 45-47 and figure 3), which reads on a memory switch. Harney teaches that the single-instruction multiple-data image processor (300) contains the block transfer controller (368) and the memory interface (370) (figure 3), which reads on memory controller and memory switch selectively connect any one or more memories out of plurality of memories to data operation unit and thereby change a memory capacity allotted to each image formation operation among the plurality of image formation operations.

8. Kawai et al. could have easily been modified with the block transfer controller and memory interface of Harney. This modification would have been obvious to one skilled in the art at the time of the invention to change a memory capacity allotted.

9. Regarding claim 3, Harney teaches that the memory interface (370) is under the control of the block transfer controller (368) (column 13, lines 45-48 and figure 3) and uses default values for the width of specified memory blocks (column 14, lines 54-57,

column 2, lines 61-65 and column 3, lines 1-5). This reads on memory controller and memory switch control plurality of data buses and change an image data transfer width allotted to each image formation operation among the plurality of image formation operations.

Regarding claim 6, claim 6 is rejected for the same reasons as claim 2.

Regarding claim 7, claim 7 is rejected for the same reasons as claim 3.

Regarding claim 9, Kawai et al. teaches of a programmable processor (image processing LSI circuit), adaptable to three image processing steps, that process image information (column 2, lines 43-45), which reads on a programmable image processing unit which processes image data as a visualized image, the image data represented by a digital signal generated based on an image, and allows realization of a plurality of image formation operations. He teaches of a data memory M1 (column 9,lines 2-4), which reads on an image data storage unit that stores the image data. Kawai et al. teaches of an image processing LSI circuit (1) which outputs a read address signal, which tells the data memory M1 to output image data V1 to the image processing LSI circuit (1) (column 2, lines 3-5), which reads on an image data storage management unit which manages access to said image data storage section. He teaches an image processing LSI circuit (1) that receives image data from data memory M1 (column 9, lines 27-30), which reads on an image data transmission of the image data between a data bus transmitting the image data and a processing unit used for the image processing conducted by said image processing unit. Kawai et al. teaches of a SIMD type first to third processing units (column 9,lines 53-54), which reads on a SIMD type

data operation unit. He also teaches that SIMD type first to third processing units generate address signal (29) for data memories 2-1 – 2-3 (column 9, lines 56-59), which reads on a plurality of memories used for the image processing conducted by said SIMD type data operation unit. Kawai et al. teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 and external memories M1 to M3 (column 9, lines 59-62), which reads on a memory controller controlling said plurality of memories. He also teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 (column 9, lines 59-62), which reads on a memory switch controlling connection of said plurality of memories. Kawai et al. shows data lines 25-1 –25-3, 26-1 – 26-3 which transfer data to the image processing units 1-1 – 1-3 (column 10, lines 43-50), which reads on a plurality of data buses for inputting and outputting the image data. He teaches of selector circuits (40-1 and 40-2) (column 10, lines 36-50 and figure 5), which reads on a bus switch controlling connection between said plurality of data buses and said data operation unit. He also teaches of a post processing portion which performs a second image processing (column 10, lines 24-27), which reads on at least one auxiliary operation unit which assists said data operation unit.

10. Kawai et al. fails to teach of the memory controller and memory switch selectively connect any one or more memories to the data operation unit.

11. Harney teaches of a block transfer controller (368) (column 13, lines 31-40), which reads on a memory controller and a memory interface (370) (column 13, lines 45-47 and figure 3), which reads on a memory switch. Harney teaches that the single-

instruction multiple-data image processor (300) contains the block transfer controller (368) and the memory interface (370) (figure 3), which reads on selectively connecting the plurality of memories to data operation unit by using the memory controller and the memory switch thereby changing a memory capacity allotted to each image formation operation among the plurality of image formation operations.

12. Kawai et al. could have easily been modified with the block transfer controller and memory interface of Harney. This modification would have been obvious to one skilled in the art at the time of the invention to change a memory capacity allotted.

Regarding claim 10, Kawai et al. teaches of a programmable processor (image processing LSI circuit), adaptable to three image processing steps, that process image information (column 2, lines 43-45), which reads on a programmable image processing unit which processes image data as a visualized image, the image data represented by a digital signal generated based on an image, and allows realization of a plurality of image formation operations. He teaches of a data memory M1 (column 9,lines 2-4), which reads on an image data storage unit that stores the image data. Kawai et al. teaches of an image processing LSI circuit (1) which outputs a read address signal, which tells the data memory M1 to output image data V1 to the image processing LSI circuit (1) (column 2, lines 3-5), which reads on an image data storage management unit which manages access to said image data storage section. He teaches an image processing LSI circuit (1) that receives image data from data memory M1 (column 9, lines 27-30), which reads on an image data transmission of the image data between a data bus transmitting the image data and a processing unit used for the image

processing conducted by said image processing unit. Kawai et al. teaches of a SIMD type first to third processing units (column 9,lines 53-54), which reads on a SIMD type data operation unit. He also teaches that SIMD type first to third processing units generate address signal (29) for data memories 2-1 – 2-3 (column 9, lines 56-59), which reads on a plurality of memories used for the image processing conducted by said SIMD type data operation unit. Kawai et al. teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 and external memories M1 to M3 (column 9, lines 59-62), which reads on a memory controller controlling said plurality of memories. He also teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 (column 9, lines 59-62), which reads on a memory switch controlling connection of said plurality of memories. Kawai et al. shows data lines 25-1 –25-3, 26-1 – 26-3 which transfer data to the image processing units 1-1 – 1-3 (column 10, lines 43-50), which reads on a plurality of data buses for inputting and outputting the image data. He teaches of selector circuits (40-1 and 40-2) (column 10, lines 36-50 and figure 5), which reads on a bus switch controlling connection between said plurality of data buses and said data operation unit. He also teaches of a post processing portion which performs a second image processing (column 10, lines 24-27), which reads on at least one auxiliary operation unit which assists said data operation unit.

13. Kawai et al. fails to teach of controlling a plurality of data buses and plurality of memories by using memory controller and bus switch.

14. Harney teaches that the memory interface (370) is under the control of the block transfer controller (368) (column 13, lines 45-48 and figure 3) and uses default values for the width of specified memory blocks (column 14, lines 54-57, column 2, lines 61-65 and column 3, lines 1-5). This reads on memory controller and bus switch control plurality of data buses and change an image data transfer width allotted to each image formation operation among the plurality of image formation operations.

15. Kawai et al. could have easily been modified with the block transfer controller and memory interface of Harney. This modification would have been obvious to one skilled in the art at the time of the invention to change the data transfer width for image formation operations.

16. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. US 5715436 in view of Harney US 5522080 as applied to claim 2 above, and further in view of Gove et al. US 6070003.

Regarding claim 11, Kawai et al. teaches of a programmable processor (image processing LSI circuit), adaptable to three image processing steps, that process image information (column 2, lines 43-45), which reads on a programmable image processing unit which processes image data as a visualized image, the image data represented by a digital signal generated based on an image, and allows realization of a plurality of image formation operations. He teaches of a data memory M1 (column 9,lines 2-4), which reads on an image data storage unit that stores the image data. Kawai et al. teaches of an image processing LSI circuit (1) which outputs a read address signal,

which tells the data memory M1 to output image data V1 to the image processing LSI circuit (1) (column 2, lines 3-5), which reads on an image data storage management unit which manages access to said image data storage section. He teaches an image processing LSI circuit (1) that receives image data from data memory M1 (column 9, lines 27-30), which reads on an image data transmission of the image data between a data bus transmitting the image data and a processing unit used for the image processing conducted by said image processing unit. Kawai et al. teaches of a SIMD type first to third processing units (column 9,lines 53-54), which reads on a SIMD type data operation unit. He also teaches that SIMD type first to third processing units generate address signal (29) for data memories 2-1 – 2-3 (column 9, lines 56-59), which reads on a plurality of memories used for the image processing conducted by said SIMD type data operation unit. Kawai et al. teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 and external memories M1 to M3 (column 9, lines 59-62), which reads on a memory controller controlling said plurality of memories. He also teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 (column 9, lines 59-62), which reads on a memory switch controlling connection of said plurality of memories. Kawai et al. shows data lines 25-1 –25-3, 26-1 – 26-3 which transfer data to the image processing units 1-1 – 1-3 (column 10, lines 43-50), which reads on a plurality of data buses for inputting and outputting the image data. He teaches of selector circuits (40-1 and 40-2) (column 10, lines 36-50 and figure 5), which reads on a bus switch controlling connection between said plurality of data buses and

said data operation unit. He also teaches of a post processing portion which performs a second image processing (column 10, lines 24-27), which reads on at least one auxiliary operation unit which assists said data operation unit.

17. Kawai et al. fails to teach of the memory controller and memory switch selectively connect any one or more memories to the data operation unit.

18. Harney teaches of a block transfer controller (368) (column 13, lines 31-40), which reads on a memory controller and a memory interface (370) (column 13, lines 45-47 and figure 3), which reads on a memory switch. Harney teaches that the single-instruction multiple-data image processor (300) contains the block transfer controller (368) and the memory interface (370) (figure 3), which reads on memory controller and memory switch selectively connect any one or more memories out of plurality of memories to data operation unit and thereby change a memory capacity allotted to each image formation operation among the plurality of image formation operations.

19. Kawai et al. in view of Harney fail to teach of a computer readable medium for storing instructions.

20. Gove et al. teaches of instructions stored on an optical disc (5001) (column 27, lines 10-23), which reads on a computer readable medium for storing instructions.

21. Kawai et al. in view of Harney could have easily been modified with the optical disc of Harney. This modification would have been obvious to one skilled in the art at the time of the invention to store image processing instructions on disc.

Regarding claim 12, Kawai et al. teaches of a programmable processor (image processing LSI circuit), adaptable to three image processing steps, that process image

information (column 2, lines 43-45), which reads on a programmable image processing unit which processes image data as a visualized image, the image data represented by a digital signal generated based on an image, and allows realization of a plurality of image formation operations. He teaches of a data memory M1 (column 9,lines 2-4), which reads on an image data storage unit that stores the image data. Kawai et al. teaches of an image processing LSI circuit (1) which outputs a read address signal, which tells the data memory M1 to output image data V1 to the image processing LSI circuit (1) (column 2, lines 3-5), which reads on an image data storage management unit which manages access to said image data storage section. He teaches an image processing LSI circuit (1) that receives image data from data memory M1 (column 9, lines 27-30), which reads on an image data transmission of the image data between a data bus transmitting the image data and a processing unit used for the image processing conducted by said image processing unit. Kawai et al. teaches of a SIMD type first to third processing units (column 9,lines 53-54), which reads on a SIMD type data operation unit. He also teaches that SIMD type first to third processing units generate address signal (29) for data memories 2-1 – 2-3 (column 9, lines 56-59), which reads on a plurality of memories used for the image processing conducted by said SIMD type data operation unit. Kawai et al. teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-1 – 2-3 and external memories M1 to M3 (column 9, lines 59-62), which reads on a memory controller controlling said plurality of memories. He also teaches of a DMA transfer control portion that controls the DMA transfer between the first to third data memories 2-

1 – 2-3 (column 9, lines 59-62), which reads on a memory switch controlling connection of said plurality of memories. Kawai et al. shows data lines 25-1 –25-3, 26-1 – 26-3 which transfer data to the image processing units 1-1 – 1-3 (column 10, lines 43-50), which reads on a plurality of data buses for inputting and outputting the image data. He teaches of selector circuits (40-1 and 40-2) (column 10, lines 36-50 and figure 5), which reads on a bus switch controlling connection between said plurality of data buses and said data operation unit. He also teaches of a post processing portion which performs a second image processing (column 10, lines 24-27), which reads on at least one auxiliary operation unit which assists said data operation unit.

22. Kawai et al. fails to teach of controlling a plurality of data buses and plurality of memories by using memory controller and bus switch.

23. Harney teaches that the memory interface (370) is under the control of the block transfer controller (368) (column 13, lines 45-48 and figure 3) and uses default values for the width of specified memory blocks (column 14, lines 54-57, column 2, lines 61-65 and column 3, lines 1-5). This reads on memory controller and bus switch control plurality of data buses and change an image data transfer width allotted to each image formation operation among the plurality of image formation operations.

24. Kawai et al. in view of Harney fail to teach of a computer readable medium for storing instructions.

25. Gove et al. teaches of instructions stored on an optical disc (5001) (column 27, lines 10-23), which reads on a computer readable medium for storing instructions.

26. Kawai et al. in view of Harney could have easily been modified with the optical disc of Harney. This modification would have been obvious to one skilled in the art at the time of the invention to store image processing instructions on disc.

Conclusion

1. Any inquiry concerning this communication should be directed to Michael Burleson whose telephone number is (703) 305-8683 and fax number is (703) 746-3006. The examiner can normally be reached Monday thru Friday from 8:00 a.m. – 4:30p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached at (703) 305-4863

Michael Burleson
Patent Examiner
Art Unit 2626
MB

KA Williams
KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER

Mlb
September 15, 2004